Design of a 1.2-V 130nm CMOS 13-bit@40MS/s Cascade 2-2-1 Continuous-Time ΣΔ Modulator

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***Abstract*– This paper presents the design of a continuous-time multibit cascade 2-2-1 ΣΔ modulator for broadband telecom systems. The modulator architecture has been synthesized directly in the continuous-time domain instead of using a discrete-to-continuous time transformation. This method results in a more efficient modulator in terms of noise shaping, power consumption and sensitivity to circuit element tolerances. The design of the circuit, realized in a 130nm CMOS technology, is based upon a top-down CAD methodology which combines simulation and statistical optimization at different levels of the modulator hierarchy. The estimated power consumption is 60mW from a 1.2-V supply voltage when clocked at 240MHz. Simulation results show 80-dB effective resolution within a 20-MHz signal bandwidth.†**

I. INTRODUCTION

Modern broadband telecommunication applications, like Very high-rate Digital Subscriber Line (VDSL) and Power Line Communication (PLC), demand Analog-to-Digital Converters (ADCs) targeting 12-14bit resolution at conversion rates of 40-80 MSamples/second (MS/s). Traditionally, these specifications have been achieved with Nyquist-rate ADCs, using pipeline or folding/interpolation topologies, because of the prohibitive sampling frequencies required by ΣΔ Modulators (ΣΔMs) [1]. However, in the last few years, the use of Continuous-Time (CT) instead of Discrete-Time (DT) circuit techniques are making possible for ΣΔMs to digitize (1-15 MHz) signals with 11-14 bit resolution [2]-[4].

In spite of achieving potentially faster operation with lower power consumption, CT ΣΔMs are more sensitive than DT ΣΔMs to some circuit errors, namely: clock jitter and technology parameter variations [5]. The latter are specially critical for the realization of cascade architectures what explains the very few Integrated Circuits (ICs) reported up to now [4].

Recent studies demonstrate that more efficient cascade CT ΣΔMs can be synthesized by using a direct synthesis method [6]. This method allows to reduce the number of analog components and to efficiently place the zeroes/poles of the noise transfer function, thus yielding to more robust architectures than using a DT-to-CT transformation [7].

This paper reports the design and electrical implementation of a cascade CT ΣΔM. The modulator architecture comprises three stages. The first two stages are a second-order topology whereas the last stage uses a first-order loop filter. All stages include 4-bit internal quantization and Non-Return-to-Zero (NRZ) Digital-to-Analog Converter (DAC) in order to attenuate the clock jitter [8]. The modulator has been synthesized directly in the continuous-time domain and no calibration is used to compensate for mismatch and element tolerances. Circuit design, realized in a 0.13μm CMOS technology and nominal 1.2-V supply voltage, has been optimized from system-level to building-block level in order to achieve the required specifications with minimum power dissipation. Simulation results demonstrate that the presented circuit can digitize 20-MHz signals with 13-bit resolution when clocking at 240MHz.

II. DESIGN CONSIDERATIONS

The modulator in this paper was designed to cope with an effective resolution over 12bit within a 20-MHz signal bandwidth. Ideally, these specifications can be achieved by different combinations of modulator order, L, number of bits of the internal quantizer(s), B, and oversampling ratio, M. However, in practice, there are some important limiting factors precluding from using some $\{L, B, M\}$ triades. These limitations impose the following design constraints:

- High-order single-loop topologies may not be feasible for the mentioned specifications because of stability issues. For that reason, only cascade architectures made up of second-order and first-order stages were considered.
- High values of B force to use linearization techniques [3] or digital calibration [2] in order to control the nonlinearity of the DAC used in the modulator feedback loop.

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- Large values of M lead to infeasible sampling frequencies in terms of power consumption.
- Last but not least, clock jitter is an ultimate limiting error that has to be addressed from the very beginning of the design process. In fact, as demonstrated in [8], the in-band noise power caused by jitter error can be minimized by proper selection of B, the sampling frequency, f_s and the modulator loop filter.

Taking into account the considerations mentioned above, an exhaustive exploration of different ΣΔM loop filters was done using SIMSIDES [9] in order to find out the optimum $\{L, B, M\}$ triade in terms of power consumption, distribution of the Noise Transfer Function (NTF) zeroes and insensitivity to clock jitter. As a result, the fifth-order ($L = 5$) cascade ΣΔM, conceptually shown in Fig.1, was selected. It consists of a 2-2-1 topology, clocked at $f_s = 240\text{MHz}$ ($M = 6$), with $B = 4$ and NRZ DAC in all stages in order to minimize the effect of jitter, that according to [8], must be below 3ps rms.

The modulator in Fig.1 can be synthesized from an equivalent DT ΣΔM. However, in order to get a functional CT ΣΔM while keeping the Cancellation Logic (*CL*) of the original DT ΣΔM, every state variable and DAC output must be connected to every integrator input of later stages [7]. The number of integrating paths, and hence of analog components, can be reduced if the whole cascaded ΣΔM is directly synthesized in the CT domain as proposed in [6]. In this paper we have selected the latter methodology, which does not only take into account the single-stage loop filter transfer functions (F_{ii}), but also the inter-stage loop filter transfer functions ($F_{ij}, i \neq j$). The latter, defined as the transfer function from y_i to the j-th quantizer (see Fig.1), are continuous-time integrating paths appearing only when the modulator stages are connected to form the cascaded ΣΔM and must be included in the synthesis methodology to obtain a functional modulator with minimum number of inter-stage paths.

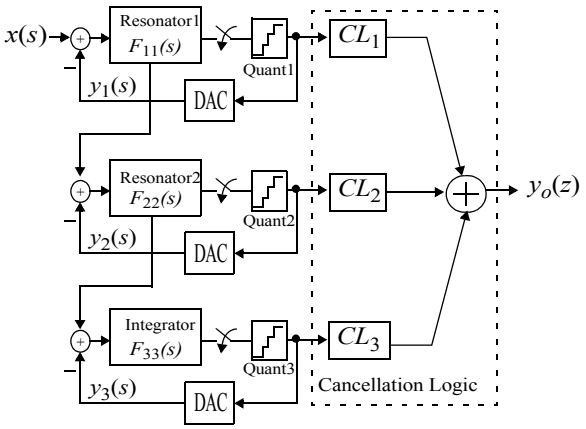

Fig. 1: Conceptual diagram of the 2-2-1 modulator.

For the modulator in this paper, the F_{ij} shown in (1) were synthesized, where $T_s = 1/f_s$ is the sampling period and $\omega_{p1,2}$ are the pole frequencies. Coefficients b_{ij} in (1) are found through an iterative simulation-based process that – starting from nominal values required to place the zeroes of the corresponding NTF – optimizes the modulator performance in terms of dynamic range and stability. For this purpose, these coefficients are varied in a range of up to ±20% around their nominal values in order to achieve the maximum Signal-to-Noise Ratio (*SNR*) while keeping stability. The partial *CL* transfer functions can be calculated from (1), giving the expressions shown in (2), where coefficients n_{ij} are shown in (3) [6].

III. MODULATOR IMPLEMENTATION

Fig.2 shows the conceptual circuit implementation of the modulator††. An RC-active front-end integrator is chosen for its better linearity whereas the rest of integrators are Gm-C [2][3]. The 4-bit quantizers were implemented using a flash ADC made up of a resistive ladder and 15 regenerative comparators. DACs were implemented by current-steering topologies. An extra feedback branch between the output and the input to the quantizer (DAC_2 in Fig.2) and two D-latches are employed in the first two stages in order to compensate for the effect of excess loop delay [2]. The first two stages are formed by a resonator which has its poles placed at an optimum position, minimizing NTF in the signal bandwidth, B_w [10]. Resistor variations can be tuned out using a combination of a discrete rough tun-

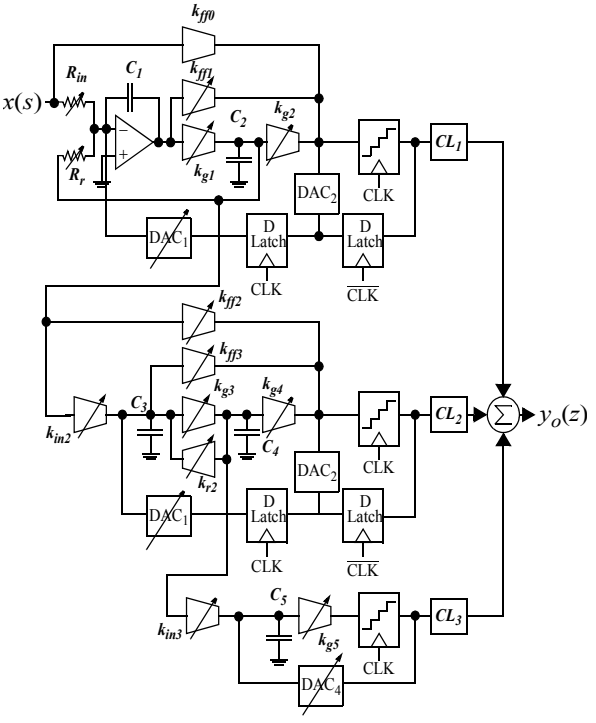

Fig. 2: Modulator implementation.

††. Although the modulator has been implemented using fully-differential circuitry, a single-ended schematic is shown here for the sake of simplicity.

$$F_{11}(s) = \frac{b_{11}s + b_{10}}{(s^2 + \omega_{p1}^2)};F_{22}(s) = \frac{b_{21}s + b_{20}}{(s^2 + \omega_{p2}^2)};F_{33}(s) = \frac{b_{30}}{s}$$
$$F_{13}(s) = \frac{b_{10}b_{20}b_{30}}{s(s^2 + \omega_{p1}^2)(s^2 + \omega_{p2}^2)};F_{23}(s) = \frac{b_{20}b_{30}}{s(s^2 + \omega_{p2}^2)} \quad (1)$$

$$CL_1 = z^{-1}(n_{14} + n_{13}z^{-1} + n_{12}z^{-2} + n_{11}z^{-3} + n_{10}z^{-4})$$
$$CL_2 = z^{-1}(n_{22} + n_{21}z^{-1} + n_{20}z^{-2}) \cdot (1 - 2\cos(T_s\omega_{p1})z^{-1} + z^{-2}) \quad (2)$$
$$CL_3 = (1 - 2\cos(T_s\omega_{p1})z^{-1} + z^{-2}) \cdot (1 - 2\cos(T_s\omega_{p2})z^{-1} + z^{-2})$$

$$n_{10} = n_{14} = \frac{-b_{10}b_{20}b_{30}}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2 - \omega_{p1}^2)} \cdot [T_s(\omega_{p1}\omega_{p2}^3 - \omega_{p1}^3\omega_{p2}) + \omega_{p1}^3\sin(T_s\omega_{p2}) - \omega_{p2}^3\sin(T_s\omega_{p1})]$$
$$n_{11} = n_{13} = \frac{-2b_{10}b_{20}b_{30}}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2 - \omega_{p1}^2)} \cdot [(T_s(\omega_{p2}\omega_{p1}^3 - \omega_{p2}^3\omega_{p1})(\cos(T_s\omega_{p1}) + \cos(T_s\omega_{p2}))) +$$
$$+ \omega_{p2}^3\sin(T_s\omega_{p1})(1 + \cos(T_s\omega_{p2})) - \omega_{p1}^3\sin(T_s\omega_{p2})(1 + \cos(T_s\omega_{p1}))]$$
$$n_{12} = \frac{-2b_{10}b_{20}b_{30}}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2 - \omega_{p1}^2)} \cdot [T_s(\omega_{p1}\omega_{p2}^3 - \omega_{p1}^3\omega_{p2})(1 + 2\cos(T_s\omega_{p1})\cos(T_s\omega_{p2})) + \quad (3)$$
$$+\omega_{p1}^3\sin(T_s\omega_{p2})(1 + 2\cos(T_s\omega_{p1})) - \omega_{p2}^3\sin(T_s\omega_{p1})(1 + 2\cos(T_s\omega_{p2}))]$$
$$n_{20} = n_{22} = \frac{-b_{20}b_{30}}{\omega_{p2}^3}[T_s\omega_{p2} - \sin(T_s\omega_{p2})]$$
$$n_{21} = \frac{-2b_{20}b_{30}}{\omega_{p2}^3}[\sin(T_s\omega_{p2}) - T_s\omega_{p2}\cos(T_s\omega_{p2})]$$

ing of the resistors (R_{in} and R_r) and a continuous fine tuning of the transconductors k_{ff1} and k_{g1}. This tuning can be also used to cancel the effect of finite Gain-Bandwidth product (GB) of the front-end opamp, due to the fact that this error can be modelled as an integrator gain error [3]. All the other transconductors can be tuned in order to keep the time constant C/g_m unchanged over C variations.

Table 1 sums up the outcome of the optimization process – entirely done in the CT domain as described in previous section. This table includes the values of loop filter coefficients, k_i (implemented as transconductances) as well as the capacitances, C_i, and resistances, R_i, used in the modulator.

The modulator was high-level sized, i.e, the system-level specifications (12-bit@20-MHz) were mapped onto building-block specifications using statistical optimization for design parameter selection and behavioral simulation for evaluation [9]. The result of this sizing process is summarized in Table 2, showing the maximum (minimum) values of the circuit error mechanisms that can be tolerated in order to fulfil the

Table 1: Loop filter coefficients of the ΣΔM

$R_{in} = R_{fb} = 1\ \text{k}\Omega$; $R_{r1} = 5\ \text{k}\Omega$,	
$C_1 = C_3 = 6$ pF $C_2 = 2.25$ pF $C_4 = C_5 = 0.75$ pF	
$k_{g1} = 500\ \mu$A/V	$k_{in2} = 800\ \mu$A/V
$k_{g3} = k_{g5} = k_{ff1} = k_{ff3} = k_{in3} = 200\ \mu$A/V	
$k_{g2} = k_{g4} = k_{r2} = k_{ff2} = 100\ \mu$A/V	
$k_{ff0} = 158\ \mu$A/V	

Table 2: High-level sizing of the ΣΔM

Front-end opamp	
GB	>580 MHz
DC Gain	>68 dB
Phase Margin	>60º
Parasitic Input Capacitance	<0.4 pF
Parasitic Output Capacitance	<0.5 pF
Diff. Output Swing	>0.5 V
Transconductors	
DC Gain	>50 dB
Diff. Input Amplitude	0.3 V
Diff. Output Amplitude	0.3 V
Third-order non-linearity	>56 dBV

required modulator performance. The data in Table 2 are the starting point of the electrical design described in next section.

IV. DESIGN OF THE MAIN BUILDING BLOCKS

The modulator has been designed in a 130nm 1-poly 8-metal logic CMOS process. Metal-insulator-Metal capacitors were used because of their good matching and linearity properties. The estimated power dissipation is 60mW from a single 1.2-V supply voltage. The ΣΔM building blocks were conveniently selected and sized according to the system-level specifications. Among the others, the most critical subcircuits are the opamps and the transconductors, described below.

A. Front-end operational amplifier

Fig.3 shows the schematic of the front-end operational amplifier together with its common-mode feedback circuit. It is a fully differential telescopic cascode topology with gain boosting. Note that p-type input scheme has been considered in order to cancel the body effect in PMOS devices – one of the mechanisms for substrate noise coupling. One of the major limitations of this topology is the output swing. However, this is not a problem in this modulator where proper system-level design reduces the front-end integrator output signal range to 0.3V. Table 3 sums up the simulated transistor-level performance of the circuit.

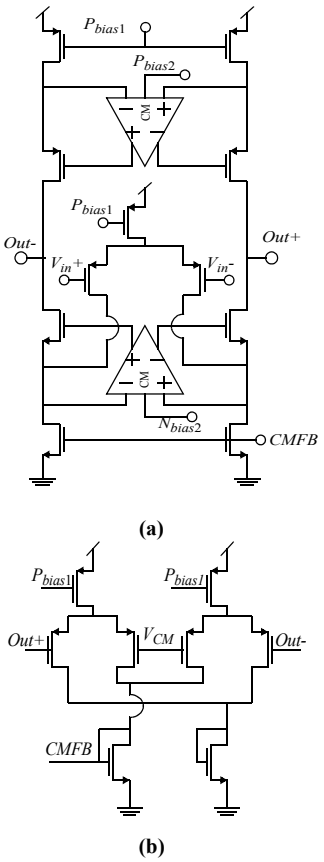

Fig. 3: Front-end operational amplifier. (a) Core. (b) CMFB circuit.

B. Transconductors

One of the main limitations in open-loop Gm-C integrators is their poor linearity. In order to tackle this problem, the transconductor shown in Fig.4, based on a quadratic term cancellation, is proposed. High-speed operation is achieved by using only feed-forward paths and by adding capacitors (C_{ff}) which introduces a high frequency zero that extends the frequency range of operation. This transconductor can be turned through the bias current, I_{tune}. In order for the tuning to be effective, each transconductance in the modulator is formed by a parallel connection of unitary transconductors of 100μA/V each. Multiple MonteCarlo simulations have been done during the design process in order to take into account the impact of mismatch on the linearity of this circuit. Table 4 shows a summary of the electrical performance.

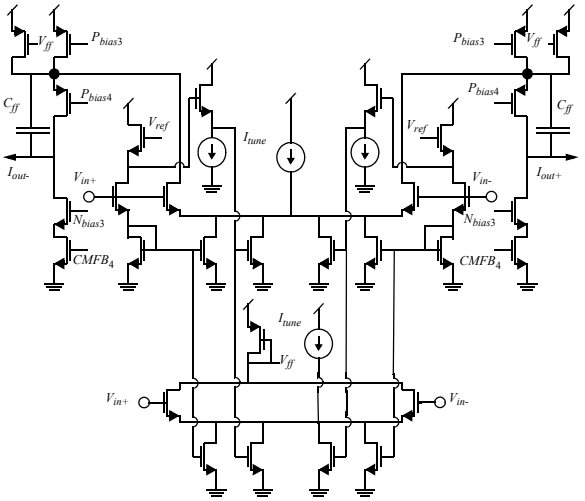

Fig. 4: Transconductor schematic.

Table 3: Transistor-level performance of the front-end opamp

GB	600 MHz
DC Gain	71 dB
Phase Margin	80º
Parasitic input capacitance	0.36 pF
Parasitic output capacitance	0.4 pF
Differential output swing	0.7 V
Power consumption	20mW

Table 4: Transistor-level performance of transconductors

DC Gain	58 dB
Diff. Input Amplitude	0.3 V
Diff. Output Amplitude	0.3 V
HD3	−57 dB
Transconductance standard deviation, σ_{g_m}/g_m	<1.5%
Power consumption	350μW

V. SIMULATION RESULTS

The modulator was simulated considering the electrical performance described above. As an illustration, Fig.5 shows the output spectrum for an input sinewave of -6.5-dBV amplitude and 1.76-MHz frequency. The maximum Signal-to-(Noise+Distortion) Ratio (*SNDR*) is 80 dB (≅ 13 bits).

In addition to the design issues discussed in previous sections, the effect of circuit tolerances and component mismatch, especially critical in cascade CT ΣΔMs, has been taken into account. The first one can be controlled in this circuit by using tuning of time constants. However mismatch error still remains. In order to evaluate the impact of this error on the performance of the modulator, maximum values of mismatch were estimated for a 130nm CMOS technology. The results of this analysis are shown in Fig.6 where the *SNR* is represented as a function of the standard deviation of the transconductances (σ_{gm}) and capacitances (σ_C). For each point of these surfaces, a MonteCarlo analysis of 150 simulations was carried out. The value of the *SNR* represented in the vertical axis of Fig.6 is obtained by 90% of the simulations for each case of σ_{gm} and σ_C. Note that even in the worst-case mismatch, the resolution is above the specified (74-dB).

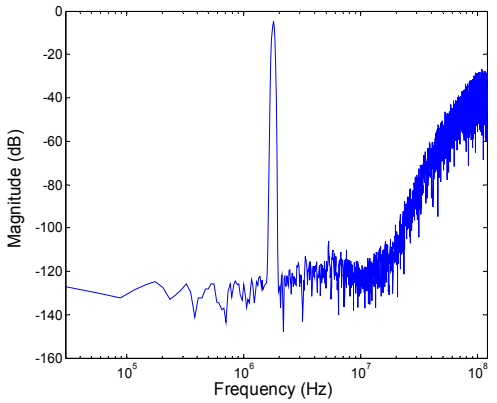

Fig. 5: Output spectrum of the modulator.

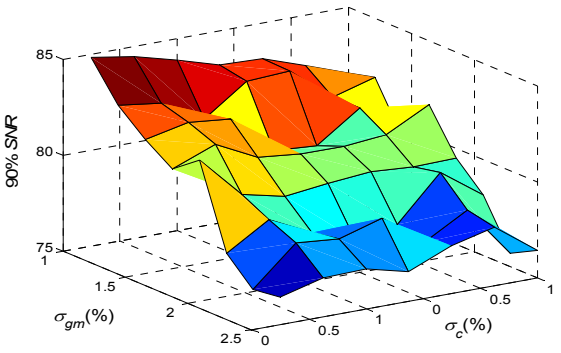

Fig. 6: Effect of mismatch on the *SNR*.

CONCLUSIONS

The design of a 1.2-V, 130nm CMOS 13-bit@20-MHz cascade CT-ΣΔM has been presented. The modulator architecture has been directly synthesized in the continuous-time domain, thus optimizing their performance in terms of circuit complexity, power consumption and sensitivity with respect to mismatch.

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